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This effort explored research and development, and deployment opportunities in the emerging disciplines of nanoscience, nanoengineering, and nanobioscience, for advanced computing architectures. The effort consisted of a multiyear, multidisciplinary effort focusing on research and development of nanocomputers systems utilizing alternative nanotechnology processing approaches that can deliver revolutionary computational capabilities crucial to maintaining technological progress. This research involved both modeling and simulations, as well as fabrication and test of prototype nanocomputing systems. Modeling results were regularly compared with experimental data as a validity check, and results were published in refereed journals and conferences.

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1. Summary

This effort explored research and development, and deployment opportunities in the emerging disciplines of nanoscience, nanoengineering, and nanobioscience, for advanced computing architectures. The effort consisted of a multiyear, multidisciplinary effort focusing on research and development of nanocomputer systems utilizing alternative nanotechnology processing approaches that can deliver revolutionary computational capabilities crucial to maintaining technological progress. This research involved both modeling and simulations, as well as fabrication and test of prototype nanocomputing systems. Modeling results were regularly compared with experimental data as a validity check, and results were published in refereed journals and conferences. The research and development proposed in this effort encompassed two primary areas of research and development. First, advances in nanoscience and technology show great promise in the bottom-up development of smaller, faster, and reduced consumed power computing systems. Nanotechnology research in this group was primarily directed towards research and development of smart learning machines that use nanotechnology to mimic information processing in nature. We are interested in not only measurements at the nanometer scale of devices and circuits that exhibit desirable information processing properties, but also incorporating hardware properties into established models focused on evolutionary computations and their applications to defined problems. Towards this end we focused on a nanodimensional crossbar computing architecture with *memristive nanoelectronics* as the active region at the crossbar junction. Second, biofunctionalized oxide nanoparticles and carbon nanotubes (CNTs) have shown tremendous promise for use in both active nanocircuits as well as nanointerconnects for ultra-high density nanocomputing systems. Research into the conduction properties of nanoparticles and carbon nanotubes, both by modeling and simulation as well as experimentally, will provide insight into the possibilities and limitations of nanoparticles and CNTs in nanocomputing architectures.

2. Introduction

The emerging revolution of nanotechnology is expected to stimulate enormous improvements in IT capabilities. Computer architectures are high on the list of technologies that will benefit from nanoscale breakthroughs in the structures, properties, and performance of microelectronics. For example, the critical feature size of Si-based, field-effect transistors has dropped below 50 nm, and yet continued reduction in transistor dimensions is expected as new nanomaterial capabilities as well as new nanoscale-centric circuit architectures are developed. However, the emerging trend in IT-focused nanotechnology development is one that looks beyond conventional CMOS technologies. It has become increasingly apparent to the IC community that the fundamental road blocks for continued enhancement of traditional approaches to transistor scaling and interconnects are rapidly being approached. Therefore, finding new computer architecture constructs – inventing and developing novel switching, memory, and interconnect technologies for processing information as well as "bottom up" based approaches to fabrication – is central to addressing the fundamental roadblocks facing IC technologies. It is anticipated that novel, nanotechnology-based, approaches to switches and interconnects will initially be implemented in conjunction with prevailing CMOS architectures. However, the full development of nanotechnology-based post-CMOS logic and memory elements are expected to result in major shifts in IC technology and redefine improvements in commercial and military information systems in ways that are anticipated to far surpass conventional CMOS. This research effort focused on exploring such novel, high-payoff, nanotechnology-based switch/interconnect paradigms based on crossbar nanoelectronic logic elements and biofunctionalized oxide nanoparticles employing the recently demonstrated phenomena of memristance [1], an enabling new nanotechnology phenomenon that is being heralded as the fourth fundamental circuit element.

Memristive nanoelectronic devices share many of the properties of resistors, as well as the same unit of measure (ohm). However, in contrast to ordinary resistors in which the unit of resistance is permanently fixed, memristance may be programmed or switched to different states based on the history of the voltage applied to the memristive nanomaterial. This gives the memristor a hysteresis property in its I-V characteristic. This can be contrasted to ordinary resistors where there is a linear relationship between current and voltage. While similar hysteresis properties have been demonstrated by magnetic materials, these require the presence of large magnetic fields for implementation which has proven to be a practical limitation to their utilization. Areas such as neuromorphic computing, signal processing, arithmetic processing, and crossbar computing are only some of the potential application areas of memristive nanomaterials.

This effort proposed to explore the synthesis, nanofabrication, and characterization of nanomaterial-based memristive nanoelectronic devices and crossbar circuit architectures.

Crossbar computer logic architectures are complex matrices of interconnected nodes that show great promise for scalability, size, weight, and power issues. In their simplest form, crossbar junctions consist of two nanowires (less than 100 nm wide) that physically "cross" each other. The junction between these nanowires is composed of a junction material with tailored transport properties. Crossbar logic elements enable massively parallel computations with the potential for a reduction in power consumption and size by up to 2-3 orders of magnitude. Crossbar computing is also tolerant to hardware defects, due to its intrinsic, network-on-chip flexibility to re-route around defects. Preliminary efforts in crossbar computing have been demonstrated by researchers at Hewlett-Packard Laboratories, in which memristive elements were used.

3. Methods, Assumptions and Procedures

Modeling

In this research and development effort, modeling and simulation were performed by co-simulation of the memristor model that was written using Verilog-A and an HSpice circuit simulator. Compact models were developed, and the memristor was modeled as a bipolar switching device. Two behavioral models were developed based on the type of electrical signal mode used to switch the device: voltage sweep mode and voltage pulsed mode. The sweep mode model of the memristive device was coded using the electrical parameters taken from electrical measurements of individual devices. The parameters were also obtained from piecewise linear approximation of its I-V curves. However, the pulsed mode model was coded using electrical parameters taken from the literature, since the pulse mode capability of the laboratory was being set up at the time.

Substrate preparation and thin film synthesis

Devices in this effort were provided by the Albany College of Nanoscale Science and Engineering under agreement FA8750-09-1-0231. The starting substrates for this effort consisted of 300 mm wafers on which $SiO_2/Si_xN_y/Si$ layers were deposited using standard chemical vapor deposition techniques. For the materials development and testing studies, Cu/Ta/TaN was deposited on the starting substrate by physical vapor deposition (PVD) as the electroplating seed, adhesion layer, and diffusion barrier, respectively. To form the Cu bottom electrode (BE), 1 µm of electroplated Cu was deposited onto the Cu seed layer. Chemical mechanical planarization (CMP) was then used to level and polish the plated Cu, smoothing the electrode surface. This Cu film served as the BE for all devices used in the development study.

Three different metal oxide films were synthesized onto the Cu BE using thermal oxidation, physical vapor deposition, and atomic layer deposition (ALD). First, TiO_x films (100 nm thick) were deposited by RF sputtering at 200 W forward power on an unheated chuck: a) in a 4.2 mTorr argon atmosphere and b) in a 4.2 mTorr argon atmosphere with an 0.1% oxygen partial pressure. These process conditions yielded a nominal deposition rate of 0.08 nm/sec. Second, HfO_x films were deposited by ALD with a chuck temperature of 250 ˚C and a chamber pressure of 0.19 Torr. Process gases used were tetrakis(dimethylamido)-hafnium(IV) as the metal-organic precursor, and a 300 W radio frequency (RF) O_2 plasma as the reactant. The target thickness of HfO_x was 50 nm. Finally, copper oxide was synthesized by oxidation (thermal and plasma) and reactive sputtering. Thermal oxidation of the copper electrode was performed at 200-400 °C in air at atmospheric pressure. Plasma oxidation was performed at room temperature

(RT) and 280 °C with an oxygen flow rate of 1-14 slm, a pressure range of 0.5-2.5 Torr, and an RF power range of 300-1000 W. Copper oxide was deposited by room temperature reactive sputtering at $1x10^{-2}$ Torr and 2000 W; the oxygen flow rate was maintained at 20 sccm, while the argon flow rate ranged from 3.5-20 sccm.

Device fabrication (for materials development/testing)

The top electrodes (TEs) for the development study were patterned using either a shadow mask or a conventional photolithography-based lift-off process. Au, Ni, Al, or Pt were deposited individually by electron beam evaporation to a final thickness of 100 nm. The resulting contacts ranged in size from 25-100 μm. For Cu_2O devices, "mesa" structures were fabricated by removing the excess Cu_2O that was not covered by the TEs. This was done through acid-based wet chemical etching of the oxide.

Crossbar fabrication

The starting substrate for this effort consisted of SiO_2/SiN/Si substrate described above. The first generation crossbar devices were fabricated using a damascene copper via process. Vias were etched into the SiO_2 layer using optical lithography and a reactive ion etch process. Cu/Ta/TaN was deposited by PVD into the vias, to act as a diffusion barrier and a seed for electroplating. Copper was then electroplated into the vias and CMP was used to remove the Cu overburden and planarize the wafer surface. The HfO_x layer was deposited using the ALD parameters from above; the target thickness of HfO_x was 50 nm. Second generation crossbar devices were fabricated utilizing a similar SiO_2/SiN/Si starting substrate. The bottom Cu electrodes were no longer based on a via-based process and instead were defined using electron beam lithography. The HfO_x for this generation crossbar was deposited by room temperature PVD to stop the Cu from migrating into the overgrown HfO_x. For both crossbar generations, the top electrode fabrication was performed using electron beam lithography.

Film and device characterization

X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) were performed for depth profiling and chemical analyses. Scanning electron microscopy (SEM), atomic force microscopy (AFM), and transmission electron microscopy (TEM) were employed to analyze the microstructure of the resulting films. X-ray diffraction (XRD) was utilized to determine the phase(s) present. Switching characteristics were investigated using sweep based current voltage (I-V) electrical measurements on an Agilent B1500A semiconductor parameter analyzer. Samples were mounted on a Cascade M150 vacuum chuck probe station in the AFRL/RI Nanotechnology Group's in-house characterization lab in Bldg. 3, and contacted with tungsten probes attached to Cascade DCM208 micro manipulators.

4. Results and Discussion

4.1 Key Accomplishments

As described above, this project focused on several key areas, including 1) modeling and simulation of crossbar/memristor circuits, as well as development of metal oxide materials for memristive circuits. The following results and discussion section describes, in detail, how each of these two tasks was performed, and the key results that were generated.

The specific tasks of the project included:

4.2 MEMRISTIVE CROSSBAR NANOCIRCUIT MODELING AND SIMULATION

4.3 MATERIALS DEVELOPMENT AND TESTING

- 4.3.1 Metal oxide materials evaluation
- 4.3.2 Evaluating the influence of copper on device properties
- 4.3.3 Alternative metal oxide fabrication methods development

4.2 Memristive crossbar nanocircuit modeling and simulation

Rationale:

Memristive devices offer a multitude of applications in computing. For example, ITRS recommends that redox-type memristors should be the subject of increased research/commercial development efforts to replace or supplement the current memory technologies, SRAM, DRAM, and Flash, as they approach their scaling limits [2]. Other applications that memristive devices are suited for include FPGA [3], encryption [4], and neuromorphic computing [5].

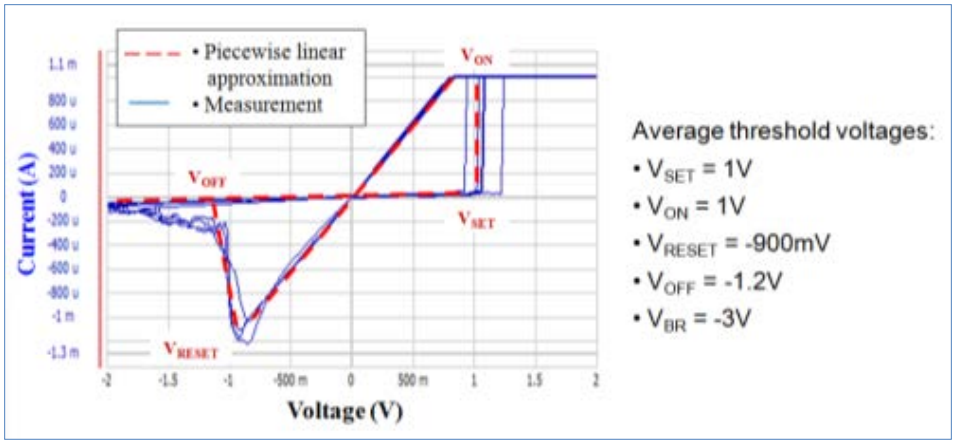
Therefore, an understanding of how a novel device, like the memristor, behaves and performs in conjunction with other devices, like CMOS, is crucial in assessing the device's performance and functionality in those architectures and circuits. This can be achieved by developing models and by performing simulations. Modeling and simulations can also serve as a guide in the fabrication and design efforts. They can provide a better understanding on the impact of parameters such as material choice, memristive junction configuration, and device dimensions on performance.

Results:

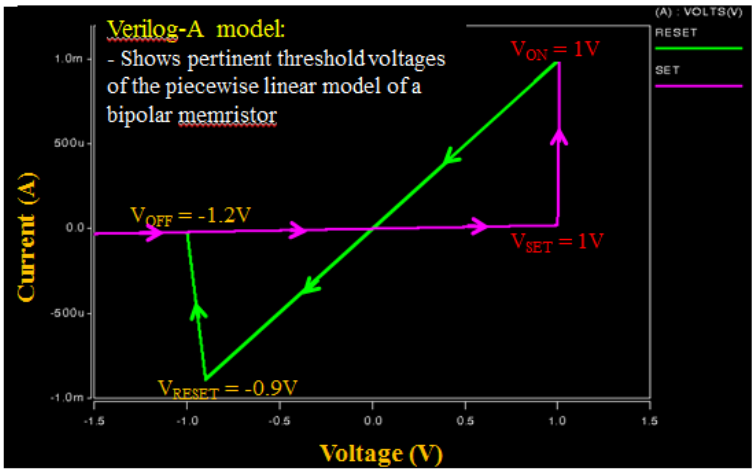
Sweep mode model

The sweep mode model written in Verilog-A as discussed above was verified using an HSpice simulation of an individual memristor. Subseqently, the model was compared with data from an actual memristive circuit.

As discussed above, the behavioral model for sweep mode was taken from electrical measurements of individual memristive devices, with its I-V curves approximated with piecewise lines (Figure 1). These parameters were then encoded into the Verilog-A model to replicate the I-V characteristics of the device operated in sweep mode. Figure 1 (a) shows the I-V curve of the model from the HSpice simulation of the individual device superimposed over actual data. From this figure it can be seen that the simulation I-V curve replicates that of the linearly approximated I-V curve from measurements, with the correct threshold voltages that were encoded into the model. This shows that the model can be used to simulate the memristor with other electrical components, such as transistors, in more complicated architectures using HSpice.



a)



b)

Figure 1 HSpice model validation of the sweep mode model written in Verilog-A. A) Sweep mode measurements taken from an individual device and its corresponding piecewise linear approximation, B) HSpice validation of the sweep model written in Verilog-A.

Pulse mode model

The sweep mode model was created to replicate the full I-V profile of a memristive device. In theory, there are an infinite number of states between the minimum and maximum resistance value afforded by a memristive device. In practice, one will not want to merely cycle a device, but stop at certain states, or resistance values, along the way. In the case of CMOS, memristive devices would be driven by pulses not DC sweeps. In light of this, a new model had to be created to account for an arbitrary pulse height and duration.

Due to the lack of empirical data, it was necessary to appeal to memristive device theory to develop the model. Memristance relates charge to flux. It is then natural to

surmise that the switching event may be triggered by satisfying an electric flux threshold, as opposed to meeting a threshold voltage. In such a model, a switching event threshold for electric flux, the time integral of the applied voltage, was set and the history of applied voltage and duration was compared to this threshold. Once the threshold is met, the model set the device. In a similar manner, through using the opposite voltage polarity, the device would reset.

To reiterate, the sweep mode model operated upon a threshold voltage switch mechanism, since the applied signal was supplied with the intent to fully set or reset the device. Under an arbitrary pulse scheme, this method could not readily be applied. Thus, based upon the flux threshold switching hypothesis, a low voltage pulse of long duration, a high voltage pulse of short duration, and a medium voltage pulse applied repeatedly were all capable of transitioning the memristive device to the low resistance state provided the flux threshold was attained. Figure 2 shows the results of a Matlab model simulation of a set operation for a single pulse, (a) – (c), and a pulse train, (d) – (f). In particular, for single-pulse programming, only two resistance states, HRS and LRS, are observed in the I-V plot, (c). However, for a pulse train, multiple intermediate states are observed in the I-V plot, (f).

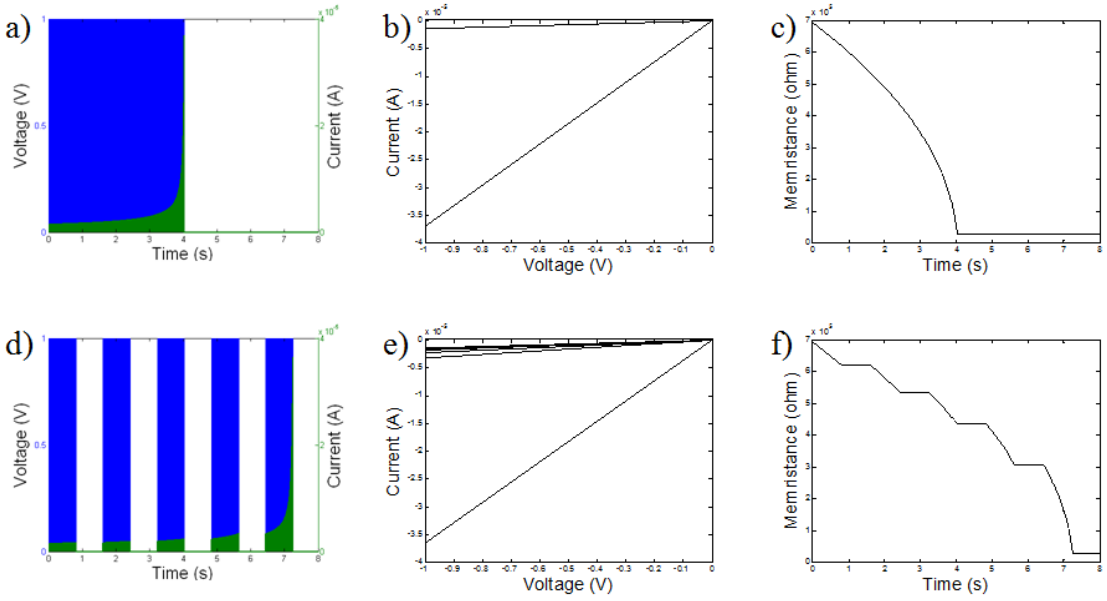


Figure 2 Matlab simulation results of a set operation via a single pulse, a)- c), and a pulse train, d) - f).

It is this repeated pulse programming that required additional thought. In the sweep mode model, there were two resistance states to operate at, LRS and HRS. For the pulse mode model, the simulated device had to be able to achieve intermediate states. As a proof-of-concept, a piece-wise linear model was employed where resistance of the memristor would change in a linear fashion. Such an approach was supported by the few

pulse-operation papers available in the literature [6-7]. As the resistance approached its maximum value, the overall change upon device behavior was minimal, whereas, for a device approaching the minimum value, the decrease in resistance was very gradual before reaching the lower limit abruptly. Such behavior is generally consistent with a linear resistance change.

In the end, the operational parameters of this model included the minimum and maximum resistance values and the threshold flux value for both set and reset operations. An example of voltage and pulse duration on the set and reset were included to determine the rate of resistance change per time step used in the simulation.

As with the sweep mode model, the pulse mode model was translated into Verliog-A to run in HSpice. Two simulations were performed. The first one was to show that providing pulses would fully switch the device from the HRS (maximum resistance) to LRS (minimum resistance). The second simulation was to show the effect of providing an arbitrary set of pulses that would enable partial switching. Figures 3 and 4 are comprised of three graphs each, in which the top graph shows the voltage pulse applied, the resulting current response is the shown in the middle graph, and the change in resistance over time is shown in the bottom. Figure 3 shows the switching response of the device when provided with set and reset pulses as well as read pulses.

As previously mentioned, these pulses should be sufficient enough to completely switch the device from HRS to LRS. As can be seen for the Set process, the resistance abruptly decreases as it reaches the threshold and then gradually changes to the LRS at the end of the pulse. The Reset process is triggered as the negative threshold voltage is reached. A linear change of resistance is then seen as it goes from the LRS to the HRS. The read pulse provided after each switching event did not trigger further resistance changes, and shows the resistance state after the switching process. Figure 4 shows that response of the device when biased with a shorter, 50 ns pulse, instead of the 110 ns pulse in Figure 3. As the resistance plot at the bottom of Fig. 4 shows, the resistance starts off in HRS. Once triggered with the voltage pulse, the device begins to decrease in resistance towards the LRS. The short pulse is only able to reduce the resistance to one of a number of intermediate resistance levels between HRS and LRS, $R_{intermediate_i}$. By providing another set of pulses which satisfies the required flux, the low resistance state, LRS, was eventually achieved. Proceeding from LRS to HRS afterwards shows a similar trend: several pulses are needed to completely switch the device from LRS to HRS.

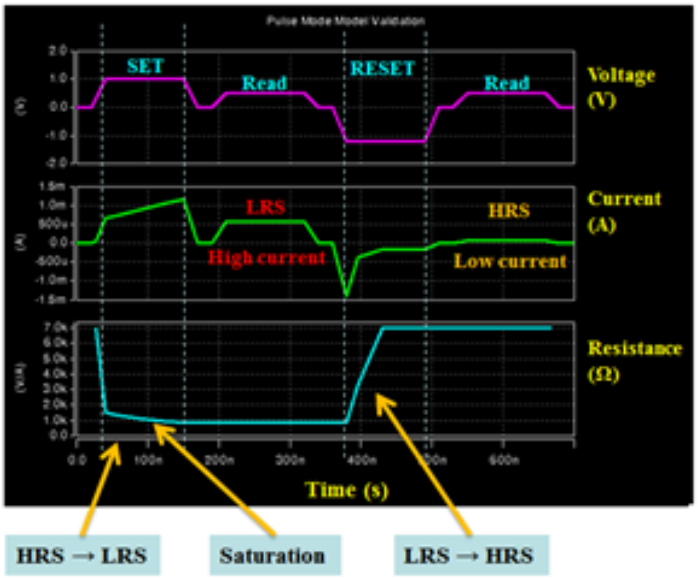


Figure 3 Pulse mode model demonstration of full cycle memristive switching using Verilog-A and HSpice, where V_{SET} = 1 V, V_{RESET} = -1.2 V, t_{SET} = t_{RESET} = 110 ns, R_{SET} = 3 kΩ, and R_{RESET} = 7 kΩ.

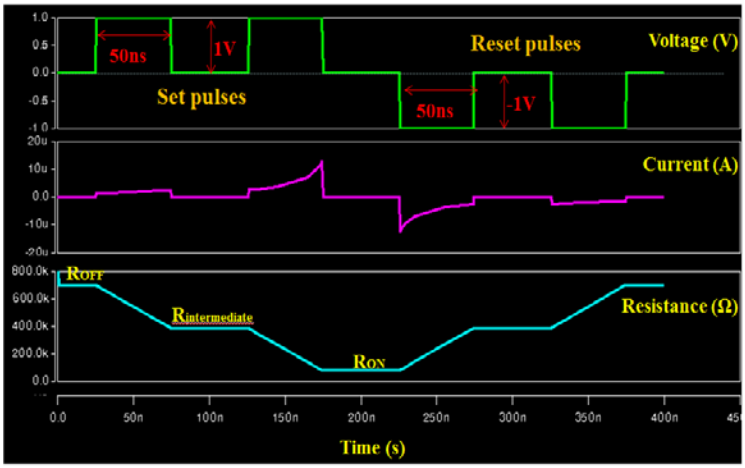


Figure 4 Pulse mode model demonstration of switching via multiple pulses, in this case two, to effect a full set or reset operation.

The pulse mode memristor model highlighted several issues that would need to be addressed. In the first, repeated DC sweeps at sub-switching voltages did not cause fabricated devices to switch as the electric flux threshold for switching events hypothesis predicted. Rather, the devices appeared to have a threshold voltage requirement. Additionally, the change in resistance in fabricated devices was not linear but rather abrupt. Numerous intermediate states as predicted in the model are rarely observed in practice.

Conclusions from memristive crossbar nanocircuit modeling and simulation:

Developing memristor models for circuit simulations is important in the design of large-scale systems in order to assess functionality and performance. We have employed behavioral modeling by approximating the I-V characteristics of actual memristive devices using piecewise linear curves and then taking the electrical parameters from them. The models are then encoded using the Verilog-A hardware description language, which was then linked to HSpice during circuit simulations. Two models, sweep mode and pulsed mode, were developed. Only the sweep mode model was validated and compared using both the simulation and actual measurements. It was shown that the sweep mode model effectively replicated the I-V characteristics of the curves taken from actual measurements. The pulse mode model, even though not validated yet through actual measurements, provided an insight on how the device may behave when stimulated using pulsed signals. For flux dependent switching devices, the model showed that full switching of the memristor is accomplished when provided with sufficient voltage and time to switch; otherwise, only partial switching is achieved.

The current models are still quite simple, and a lot of improvements still need to be done. In the future, it will be necessary to use the models to simulate larger systems and assess how well they perform. The models can also be updated to include other effects such as temperature. In doing so, the model can encompass a wider range of operations. Empirical models are quite useful when the physical mechanisms governing the memristor are not well understood; however, it will be better to incorporate the physics of the devices once this understanding is available. While physical models can improve the accuracy of the simulations, the associated computational costs might limit its usefulness in larger circuits. This trade-off will need to be considered when choosing the appropriate model to use.

4.3 Materials Development and Testing

4.3.1 Metal oxide materials evaluation

Rationale:

Metal oxide based resistive memory devices can be fabricated using a wide array of metal oxide insulator/metal electrode combinations. To date, few studies have rigorously compared devices fabricated from multiple electrode/insulator combinations. Those studies that have compared devices with different electrode/insulator combinations show that the choice of electrode plays a large role in the switching characteristics of the resulting MIM devices. Kim, *et al.* used several different metal TEs for TiO_x–based devices, including Pt, Au, Ni, Al, and Ti [8]. When using Pt and Au electrodes, both bipolar and unipolar switching was observed; but Ag devices exhibited only bipolar behavior. Further, devices fabricated with Ti TEs were not able to be switched, while Ni and Al TEs resulted in unstable switching behavior. Similar trends were observed by Vallee, *et al.* for HfO_x-based devices in which the switching behavior for Pt TEs was superior to Au and $WSi_{x(x>2)}$-based TEs [9]. Another study using HfO_x-based devices showed that the conductivity of the low resistance state (LRS) was related to the choice of TE material, and the heat of formation for oxidation of that material [10].

Clearly, the choice of metal oxide and electrode materials for resistive memory devices is important for their resulting electrical behavior. In this study, we chose to investigate several metal oxide/electrode combinations in an attempt to gain a broader understanding of their effects on resistive switching behavior. Cu_2O, HfO_x, and TiO_x oxides were formed on copper BEs, followed metallization with four different TEs (Ni, Au, Al, and Pt). Current-voltage measurements were then performed to characterize the switching behavior (unipolar, bipolar, non-polar), resistance ratio (R_{OFF} vs. R_{ON}), and approximate set/reset voltages.

Results:

TiO_x devices exhibited a wide range of electrical characteristics which were dependent upon both the TiO_x deposition method used and the TE material. In general, TiO_x deposited in an Ar-only atmosphere yielded devices with more repeatable switching behavior than TiO_x deposited in an Ar/O_2 atmosphere. In particular, devices deposited in an Ar/O_2 atmosphere with Al and Ni TEs exhibited diode-like behavior and could not be switched from HRS to LRS. Devices fabricated with Au and Pt TEs yielded the most consistent performance for both the Ar and Ar/O_2 deposition conditions. These devices had similar resistive switching properties with set voltages of ~0.7 V, reset voltages less

than -0.4 V, and R_{OFF}/R_{ON} ratios of ~10^6. Interestingly, devices with Al and Au TEs exhibited unipolar switching behavior (turn-on and turn-off in the same voltage polarity) while devices with Ni and Pt TEs exhibited bipolar behavior (set and reset with opposite voltage polarity). Characteristic I-V curves from TiO_x devices with Ni and Al TEs are shown in Figure 5.

Our devices behaved differently than those described in previous studies using TiO_x as the metal oxide. Kim *et al.* [8] reported both unipolar and bipolar behavior for Pt and Al TEs, while we observed only unipolar behavior for Al and only bipolar behavior for Pt. This group further showed that Ni and Al TEs yielded devices with unstable switching behavior, while we had mixed results for these electrode materials, partially dependent upon the deposition conditions of the TiO_x. Some of these differences may be due to the fact that Kim's devices used Pt BEs, while Cu BEs were used in our devices. However, since the BE material was not varied in our experiments, we cannot determine the overall effect it has on switching behavior.

A distinguishing feature of the TiO_x-based devices was contact bubbling and delamination (see inset in Figure 5 (b)). This phenomenon is well documented by multiple research groups [11-12], and has been suggested to be the result of oxygen released from the bulk TiO_x. Contact bubbling was most pronounced when Au was the TE. Ultimately, contact bubbling will limit the integration of TiO_x-based memory devices with CMOS systems if this issue is not addressed.

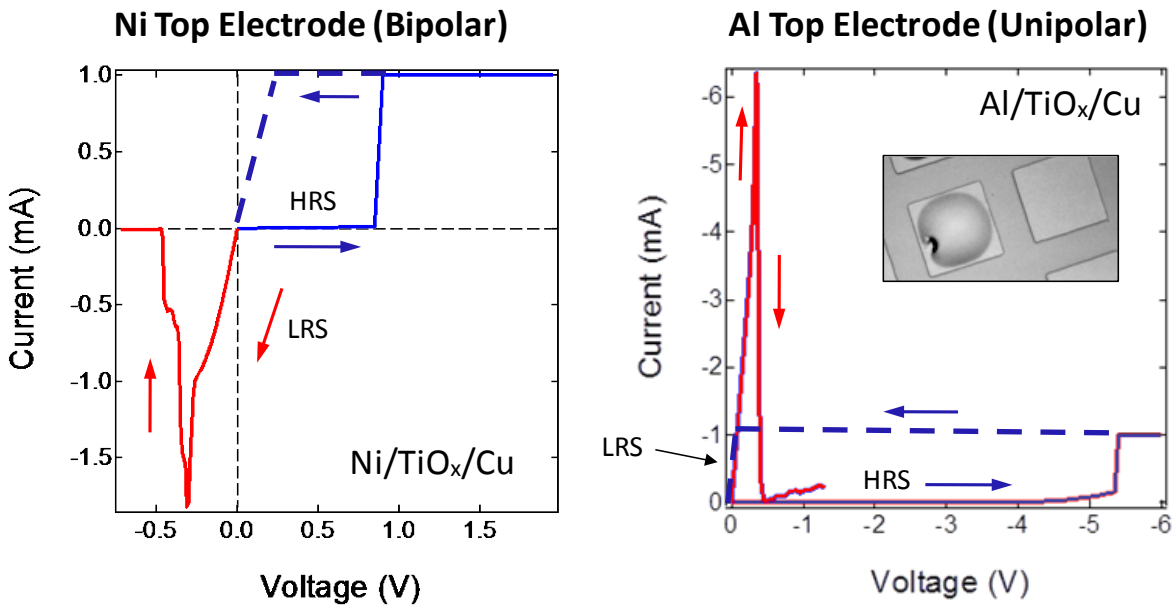
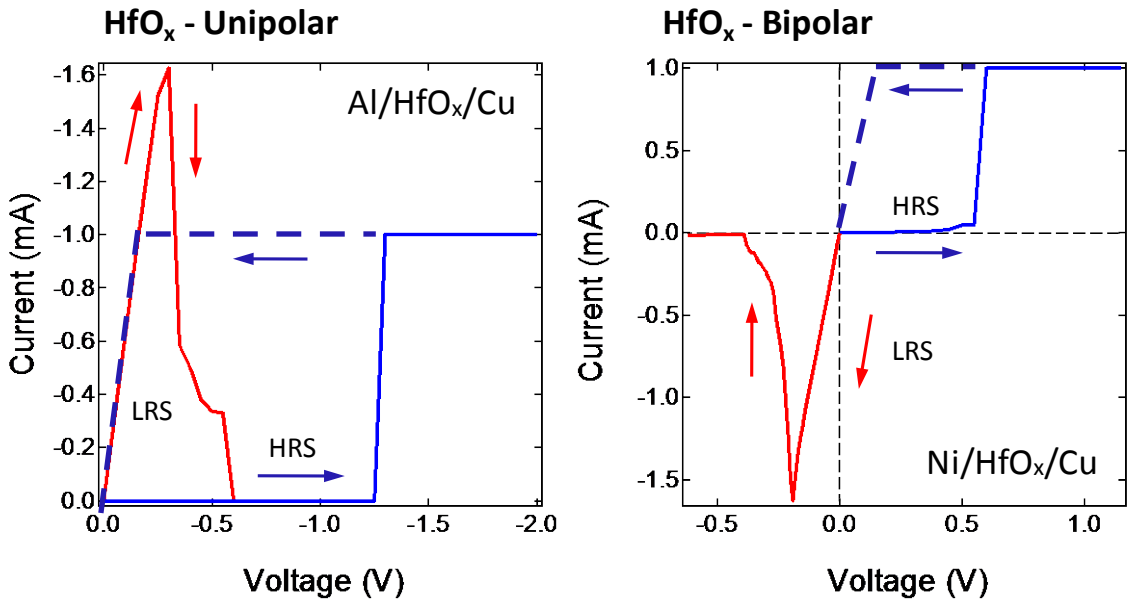


Figure 5 Current-voltage plots showing both bipolar, a), and unipolar, b), switching behavior for TiO_x devices. Bipolar behavior was observed when Ni top electrodes were used, while unipolar behavior was observed for devices with Al top electrodes. Top electrode bubbling and delamination (b), inset was observed for all TiO_x devices, regardless of top electrode material.

HfO_x-based devices exhibited non-polar switching behavior independent of the TEs and without the need for a forming voltage. Non-polar behavior was exhibited by the ability to switch in both a unipolar and bipolar manner, regardless of TE material. In addition, set voltages less than +/-1 V and reset voltages on the order of +/-500 mV were observed with average R_{OFF}/R_{ON} ratios of 10^8. Examples of I-V switching behavior for HfO_x-based devices are shown in Figure 6. This figure shows data from two different devices (one with a Ni TE and one with an Al TE). Both unipolar and bipolar switching were observed for both of these TE materials.

Unipolar, bipolar, and non-polar switching behavior have all been observed for HfO_x-based devices [9-10]. Similar to the TiO_x results (above), this could potentially be due to the Cu BE used in this study. Cu may well play a role in the switching behavior that is observed for some of these devices, and other work by our group has shown that Cu may diffuse to the upper surface of the HfO_x during the deposition process [13]. This could have significant influence on the switching behavior of these devices.



a) **b)**

Figure 6 Current-voltage plots showing both unipolar, a), and bipolar, b), switching behavior for HfO_x devices. Switching behavior for HfO_x devices was independent of electrode material.

Cu_2O device behavior was strongly dependent upon TE material, and these devices did not demonstrate resistive switching behavior with either Au or Ni TEs. Further, only "mesa" devices exhibited consistent switching behavior. Devices that contained a continuous thermal oxide layer showed diode behavior independent of the top electrode. Mesa devices fabricated with Pt and Al TEs exhibited only bipolar switching behavior and repeated attempts at unipolar switching were unsuccessful. Current-voltage characterization indicated that the Cu_2O devices with Al TEs switch more consistently (at similar set and reset voltages) than those fabricated with Pt TEs. For the Cu_2O devices with an Al TE, set voltages ranged from 1.5-2.5 V, and reset voltages were less than -1V. The R_{OFF}/R_{ON} ratio for these devices ranged from 10^3-10^4. An example I-V curve is shown in Figure 7 for a Cu_2 device with an Al TE.

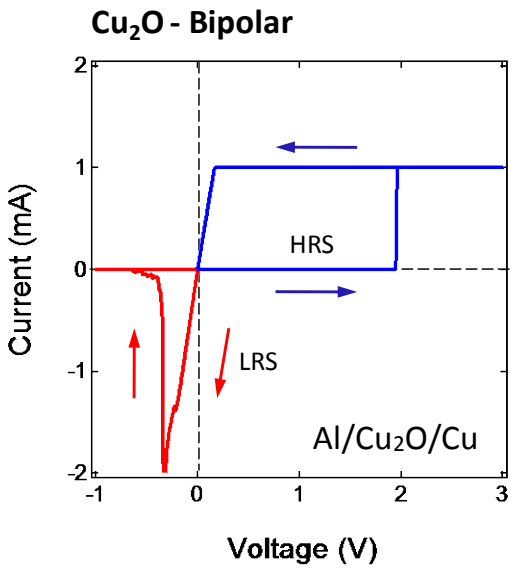


Figure 7 Current-voltage plot showing bipolar resistive switching behavior of Cu_2O based devices with Al top electrodes and Cu bottom electrodes.

In summary, devices with three types of metal oxides (Cu_2O, HfO_x, and TiO_x) demonstrated resistive switching characteristics which were highly dependent upon the type of material used for the TE. The results from this study are compiled in Table I, below. This work shows that TE selection is an important factor for determining the resistive switching properties of MIM devices, and that this factor alone can determine switching polarity. Notably, not all TE / metal oxide combinations yielded switchable devices. Our work did not examine the role of the BE, since all devices tested used Cu BEs. Ongoing efforts in the AFRL/RI Nanotechnology Group are focused on determining the role of BE on resistive switching characteristics, since this electrode could also have an important role in determining other aspects of switching behavior, including the set/reset voltage and R_{OFF}/R_{ON}.

Table I. Summary of results from the metal oxide/top electrode survey.

Oxide	Synthesis	Top Electrode			
		Al	Au	Ni	Pt
Cu_xO	Thermal Oxidation	Bipolar	Diode	Diode	Bipolar
TiO_x	PVD (Ar)	Unipolar	Unipolar	Bipolar	Bipolar
	PVD (Ar and O_2)	Diode	Unipolar	Diode	Bipolar
HfO_x	ALD	Non-polar			

Conclusion from Metal Oxide Materials Screening:

Both the metal oxide insulator and the metal TE independently impact the resistive switching properties, in particular the switching polarity.

4.3.2 Evaluating the influence of copper on device properties

Rationale:

Hafnium oxide has been previously studied as the active layer in resistive memory devices by multiple groups. These investigations have demonstrated devices with stable, long-term read/write endurance [14-16], low switching energy [17], and high on/off ratios [15]. Previous work has shown the effects of Cu on the performance of HfO_x based resistive memory. HfO_x is intentionally doped either via a Cu layer inserted between the HfO_x [15] or using Cu as a top electrode as a reservoir of metallic ions. Through either method, Cu is thought to form conductive filaments during switching [16]. One principal result from the preceeding oxide-electrode study was the nonpolar switching behavior of the HfO_x devices. Since copper is a mobile atom in this oxide material and is the *de facto* bottom electrode in this research, the role of copper doping on the switching properties of HfO_2 films created by atomic layer deposition was investigated.

Results:

The XPS depth profile of an as-deposited HfO_x film measured in collaboration with Albany CNSE under agreement FA8750-09-1-0231 is shown in Figure 8 (a). There are three noteworthy points from these data. First, the profile shows that the HfO_x is not stoichiometric because the [O]/[Hf] ratio is equal to 1.1. Second, there is a significant (unintentional) copper impurity concentration present in the HfO_x. The latter is on the order of five atomic percent throughout the portion of the HfO_x layer that was analyzed. Even more surprising is the increase in the copper concentration at the beginning of the profile. The copper concentration in this region varies from a maximum of 60%, to 32% at the sample surface. Concurrently, the oxygen profile varies before stabilizing at 50% in the HfO_x layer. These data clearly indicate the final point; a copper oxide layer of varying stoichiometry resides on the surface of the HfO_x. The presence of this Cu_xO layer has not been reported previously. In addition, this layer could play a significant role in the electrical properties of these devices because Cu_xO has also been shown to be a resistive memory material [18].

In order to achieve better depth resolution and sensitivity to trace concentrations, SIMS was then employed in collaboration with Albany CNSE under agreement FA8750-09-1-0231 to characterize the copper within the HfO_x. Figure 8 (b) shows the results from a SIMS analysis of a $Pt/HfO_x/Cu$ device structure. This device was profiled "as fabricated" and was therefore not influenced by any electrical bias before analysis. At the uppermost interface (Pt/HfO_x), the Cu signal peaks along with O, indicating the presence of the Cu_xO layer. The estimated thickness of the Cu_xO is less than 20 nm.

The accuracy of this thickness measurement from SIMS is limited by the differential sputtering rates of the materials in the MIM device structure. After the peak concentration of Cu at the interface, the concentration declines continuously, until another spike in Cu is observed at the beginning of the bulk Cu electrode. This is not an expected result. Normally, in a bulk diffusion process, we would expect a decreasing concentration of Cu from the bulk bottom electrode to the surface, the opposite of what is observed. Further investigation is therefore needed to understand the profile of Cu observed in these structures as well as the trace concentration of Pt observed throughout the HfO_x region. Subsequent X-ray diffraction studies (not shown) indicated that the bulk structure of the film is amorphous, although this does not preclude regions of nanocrystallinity.

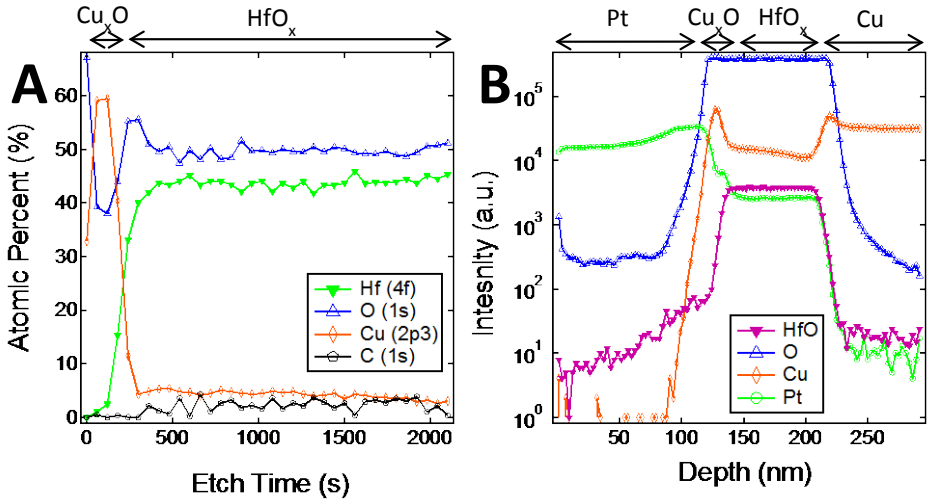


Figure 8 a) XPS depth profile of ALD HfO_x on Cu. The uppermost portion of the profile shows Cu_xO layer formation. b) SIMS depth profile of a Pt/HfO_x/Cu MIM device, confirming the presence of an interfacial Cu_xO layer.

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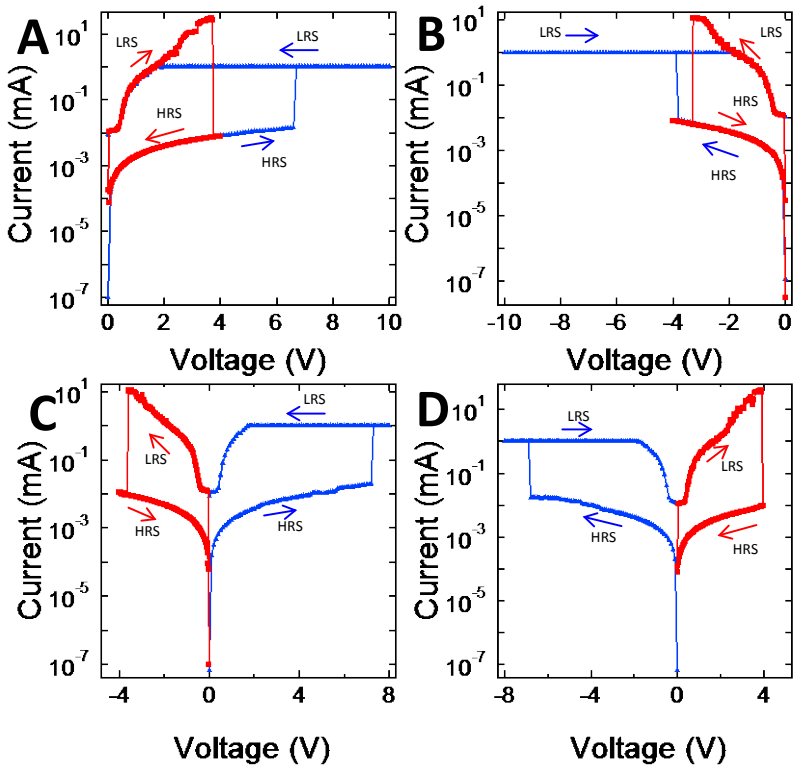


Figure 9 Current voltage measurements of a Pt/HfO$_x$/Cu MIM. a) - b) Unipolar operation, independent of bias direction. c) - d) Bipolar operation, with set voltage in both positive and negative polarity.

Top electrode biased current voltage measurements show both unipolar, Figure 9 (a)-(b), and bipolar, Figure 9 (c)-(d), resistive switching behavior. This behavior is known as "non-polar" resistive switching, in which only the magnitude of the voltage, not the polarity, dictates switching. The device in Figure 9 exhibited a change in resistance state during the application of a voltage sweep [$0 \rightarrow V_{set}$] with V_{set} = |6-8| V. (Note: all sets used a 1 mA current compliance which was found to be the optimal value for these devices). Transitions from a LRS to HRS were observed with a follow-up voltage sweep [$0 \rightarrow V_{RESET}$] of either polarity, with no current compliance. V_{RESET} was consistent during each cycle at around |4| V. Previous studies report that HfO_x can behave as a unipolar [17], bipolar [16], or non-polar [14-15] switch. To the best of the our knowledge, this is the first report of ALD HfO_x on Cu for resistive memory. Our process shows a significant, 5% Cu doping, very similar to the work of Wang *et al.*[15], who used a similar Cu doped HfO_x MIM ($Cu/HfO_x/Cu/HfO_x/Pt$) structure where a thin Cu layer was deposited between the HfO_x to dope it, in an attempt to improve switching performance. The Wang *et al.* group [15] attributed the non-polar switching phenomena to the formation of Cu rich filaments, which form a low resistance conduction pathway.

Our results of non-polar switching behavior agree very closely with the work of Wang *et al.* [15]. The unintended formation of the Cu_xO layer by ALD, does not appear to influence the root electronic mechanism, whether it be filamentary in nature, or an undiscovered phenomenon causing the non-polar resistive switching in HfO_x.

Devices exhibited sweep mode endurance of around 2-15 cycles before failure (as shorts). This is likely due to the large quantity of power applied to the device during sweep mode measurements. In order to alleviate this stress we employed pulse based measurements for the set operation. Figure 10 (a) shows the reset sweep measurements for multiple cycles after a pulsed set (pulse width of 10 µs with a pulse height of 3 V). There is no current measured for the first -0.7 V of the reset curve, due to the bias scheme of the device in the 1T1R configuration (Figure 10 (b)). In this configuration, a critical field is needed to overcome the drain to well junction barrier. Pulse based sets greatly improved the endurance of the devices (>30 cycles), and future work will include a complete set and reset pulsing study.

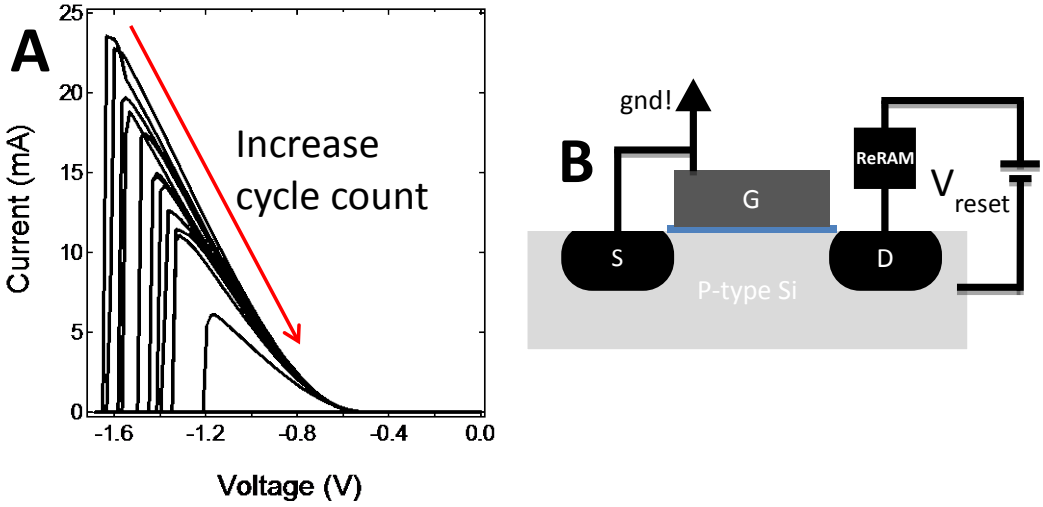


Figure 10 a) Sweep mode I-V for reset, of a Ni/HfO_x/Cu MIM. Set operation carried out by application of pulse. b) 1T1R configuration for reset I-V sweep.

Conclusions from evaluating the copper influence studies:

XPS and SIMS depth profiles showed that a ~20 nm thick Cu_xO layer formed at the surface of the HfO_x. I-V data show non-polar resistive switching properties independent of top electrode material. Use of pulse mode measurement in a 1T1R configuration greatly improved endurance, by reducing total power dissipation stress during the set operation. Preliminary work on nanoscale via-based devices show bipolar switching characteristics with high I_{on}/I_{off} of 10^{10}. However, a large amount of Cu depletion at the surface of the via due to the ALD of HfO_x.

4.3.3 Alternative metal oxide fabrication methods development

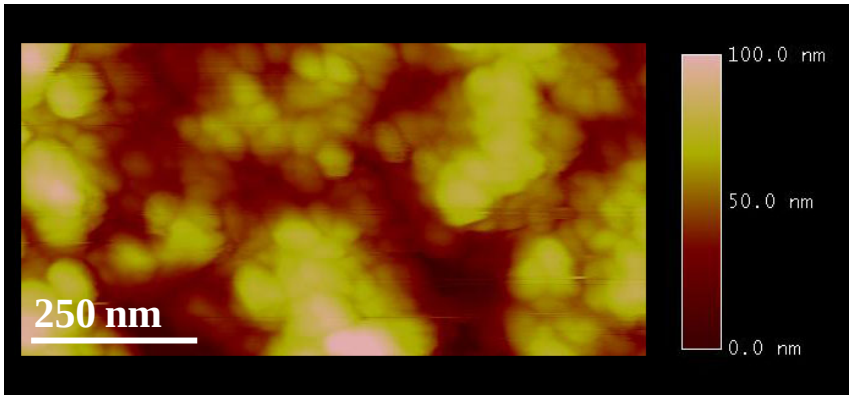
Rationale:

Copper oxide is one of the transition metal oxides that exhibits resistance-based memory. Copper oxide RMDs have been produced with R_{OFF}/R_{ON} ratios up to 10^5 [19] and endurance values of $>10^4$ write/erase cycles [19]. Data retention times of >10 years have also been predicted [20-21]. Owing to copper's ubiquitous use as an IC interconnect metal, fabricating an oxide from this material is very advantageous for resistive memory applications. In this work, a systematic investigation has been performed to determine how the oxide synthesis technique, film properties, and the device fabrication process impact the switching behavior of RMDs. Note that a novel oxygen implantation-based synthesis technique was invented as a part of this research.

Results:

Copper oxide thin films produced by thermal oxidation over the temperature range 200-400 °C exhibited rough surfaces. In collaboration with Professor Rebecca Cortez of the Mechanical Engineering Department of Union College, Figure 11 (a) shows the AFM height image of a copper oxide films synthesized at 300 °C for 60 min. The RMS (root-mean-square) roughness of the image is 32 nm. The topography of the surface is evident from the 100 nm height scale of the image. Cuprous oxide (Cu_2O) was the primary phase for all of the films produced by thermal oxidation; their XRD patterns described earlier. The majority of the devices fabricated from thermally oxidized copper exhibited a diode-like behavior as shown in Figure 11 b). The diode-like behavior was observed in as-fabricated devices and after a large increase in current, similar to the set process common to RMDs. The diode behavior did not change with time or bias conditions and thus multiple resistance states were not observed for these devices. The diode-like I-V behavior occurred independent of the top electrode used. Some devices fabricated from thermally oxidized copper with large area contacts (1 mm in diameter) exhibited bipolar switching; however, the resistance ratio (R_{OFF}/R_{ON}) was low (~1.5). The latter is due presumably to the large area of the contacts giving rise to low off-state resistance values.

a)



b)

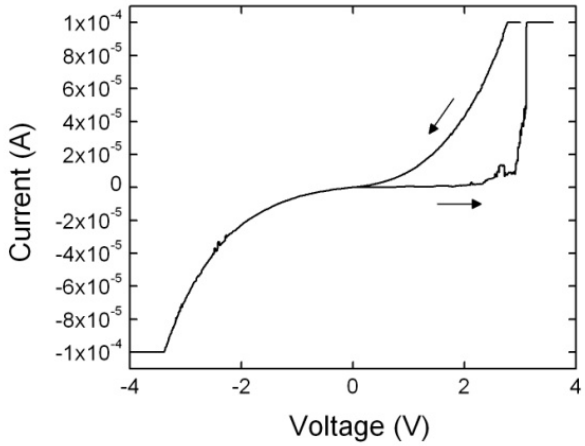


Figure 11 a) AFM height image of the surface of thermally oxidized copper (300 °C and 60 min.) and b) the diode-like current-voltage behavior from a device fabricated from the same sample with an Al top electrode (100 nm). In collaboration with Prof. R. Cortez, Department of Mechanical Engineering, Union College, Schenectady, NY.

Conclusions from alternative metal oxide fabrication study:

Copper oxide has been synthesized by thermal and plasma oxidation and reactive sputtering. Devices fabricated 1) from thin copper oxide layers and 2) into confined areas yielded the most robust switching characteristics. High oxidation rates produced copper oxide films with a defective microstructure. Voids at the copper-copper oxide interface made devices based on these films unsuitable for resistive memory applications. Further, interfacial voiding becomes much more significant as the device size decreases. This study has illustrated some of the challenges that will be encountered as copper oxide RMDs are scaled to smaller dimensions and integrated with CMOS.

4.4 Presentations and Publications

Presentations

1. N.R. McDonald, S.M. Bishop, B. D. Briggs, J. E. Van Nostrand, and N.C. Cady, "Analysis of Nonpolar Resistive Switching Exhibited by Al/Cu_xO/Cu Memristive Devices Created via Room Temperature Plasma Oxidation", International Semiconductor Device Research Symposium, Baltimore, MD, Dec. 2011.

2. B.D. Briggs, S.M. Bishop, K.D. Leedy, T. Murray, K. Dunn, R. Matyi, J.E. Van Nostrand, and N.C. Cady, "Characterization of the Interfacial Cu_xO Layer in HfO_x/Cu Resistive Memory", Physical Electronics Conference, College of Nanoscale Sci./Eng., Univ. at Albany, Albany, NY, June 2011.

3. B.D. Briggs, S.M. Bishop, K.D. Leedy, B. Butcher, R. L. Moore, S. W. Novak, and N.C. Cady, "Influence of Copper on the Switching Properties of Hafnium Oxide-Based Resistive Memory", Spring MRS 2011, San Francisco, CA, April 2011.

4. S.M. Bishop, B.D. Briggs, K.D. Leedy, S. Addepalli, and N.C. Cady, "A Survey of Metal Oxides and Top Electrodes for Resistive Memory Devices", Spring MRS 2011, San Francisco, CA, April 2011.

Conference Proceedings Articles

1. S.M. Bishop, B.D. Briggs, Z.P. Rice, S. Addepalli, N.R. McDonald, and N.C. Cady, "Fabrication and Characterization of Copper Oxide Resistive Memory Devices", *Mater. Res. Soc. Symp*. 1337 (2011) 55.

2. B.D. Briggs, S.M. Bishop, K.D. Leedy, B. Butcher, R. L. Moore, S. W. Novak, and N.C. Cady, "Influence of Copper on the Switching Properties of Hafnium Oxide-Based Resistive Memory", *Mater. Res. Soc. Symp.* 1337 (2011) 49.

3. S.M. Bishop, B.D. Briggs, K.D. Leedy, S. Addepalli, and N.C. Cady, "A Survey of Metal Oxides and Top Electrodes for Resistive Memory Devices", *Mater. Res. Soc. Symp*. 1337 (2011) 91.

Journal Articles

1. R. Cortez, J.M. Slocik, J.E. Van Nostrand, N.J. Halas, and R.R. Naik, "Electrical conductivity of cationized ferritin decorated gold nanoshells", J. *Appl. Phys.* **111** (2012) 124311.

2. N. R. McDonald, S. M. Bishop, B. D. Briggs, J. E. Van Nostrand, and N.C. Cady, "Analysis of Nonpolar Resistive Switching Exhibited by Al/Cu_xO/Cu Memristive Devices Created via Room Temperature Plasma Oxidation" Submitted to *Sol. State Elect.* (2011) In Review

5. Conclusions

This effort has resulted in crossbar resistive memory devices/memristors that can be used for future memory and logic applications. Multiple metal oxides were evaluated for integration into crossbar memristors, with hafnium oxide being the ideal candidate for future study, due to ease of integration, endurance, and performance parameters. Copper oxide is also a viable material, but fabrication and performance issues could make long-term integration of this material challenging. In addition to characterizing metal oxides deposited by thin film deposition methods, we also established a novel *in situ* fabrication method of converting metals to metal oxides. This oxygen ion beam modification method is the subject of a provisional US patent application filed during the course of this effort. This method is promising for scaled-up manufacturing of memristive devices.

The modeling and simulation efforts described in this report show that memristors in a 1T1R configuration have better performance characteristics than a simple one memristor configuration. This may have to do with current overshoot during the switching or forming steps of operation. Further, modeling shows that there may be intermediate switching states (partial switching) during pulse-mode operation. This will be explored further in subsequent efforts. Finally, we have fit some of our device data to literature-based physical models which show that our devices behave similar to what is expected for “filament” based memristors. We hypothesize that our use of a copper bottom electrode may be influencing filamenet formation, possibly by introducing a metallic copper filament into the metal oxide dielectric. Future efforts will seek to identify these filaments and to engineer the materials system for increase switching endurance, which may be highly dependent upon these filaments.

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List of Acronyms

AFM: Atomic force microscopy
ALD: Atomic layer Deposition
BE: Bottom electrode
CMP: Chemical mechanical planarization
ECD: Electrochemical deposition
FIB: Focused Ion Beam
HRS: High resistance state
ITRS: International Technology Roadmap for Semiconductors
I-V: Current-voltage
LRS: Low resistance state
MIM: Metal-insulator-metal
PVD: Physical Vapor Deposition
ReRAM: Resistive random access memory
RF: Radio frequency
RMD: Resistive memory device
RRAM: Resistive random access memory
SEM: Scanning electron microscopy
SIMS: Secondary ion mass spectrometry
TE: Top electrode
TEM: Transmission electron microscopy
XPS: X-ray photoelectron spectroscopy
XRD: X-ray diffraction
1T1R: One transistor one resistor